**DIGITAL ELECTRONICS TEST -1**

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| 1.  | Convert hexadecimal value 17 to decimal. |
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| **A.** | 2310 | **B.** | 1610 |
| **C.** | 1010 | **D.** | 2010  |

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| 2.  | Convert the following decimal number to 8-bit binary 178 |
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| **A.** | 101110112 | **B.** | 110111012 |
| **C.** | 101100102 | **D.** | 101111002 |

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| 5.  | 3. Convert binary 1001110010 to hexadecimal. |
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| **A.** | EE216 | **B.** | FF216 |
| **C.** | 2FE16 | **D.** | 27216 |

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| 4. Convert the following binary number to decimal. 011111 |
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| **A.** | 11 | **B.** | 31 |
| **C.** | 15 | **D.** | 10 |

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| Decode the following ASCII message.1010011101010010101011000100101100101000001001000100000110100101000100 |
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| --- | --- |
| **A.** | STUDYHARD |
| **B.** | STUDY HARD |
| **C.** | stydyhard |
| **D.** | study hard |

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| 6.  | Convert the decimal number 162.75 to binary. |
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| **A.** | 10100010.11 | **B.** | 11010011.01 |
| **C.** | 00111100.00 | **D.** | 10010111.11 |

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| 7. The number of bits used to store a BCD digit is: |
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| **A.** | 8 | **B.** | 4 |
| **C.** | 1 | **D.** | 2 |

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8. A number is represented in its 2’s complement form as 1100111 what is its decimal valu

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|  **A.** | -25 | **B.** | 25 |
|  **C.** | 27 | **D.** | -27 |
|  |  |

9 the parity bit to be added to the data 11110000001 to make it in to even parity

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|  **A.** | 1 | **B.** | 0 |
|  **C.** | 3 1s | **D.** | No need |

10 which of the following number system has two 0s

|  |  |  |  |
| --- | --- | --- | --- |
|  **A.** | Sign magnitude form | **B.** | 1’s complement form |
|  **C.** | 2’s complement form | **D.** | None |

11 The gray code for the binary number 111001 is

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| --- | --- | --- | --- |
|  **A.** | 100101 | **B.** | 000101 |
|  **C.** | 111010 | **D.** | None |

12 The Boolean expression suitable to the logic circuit is

 

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| --- | --- | --- | --- |
|  **A.** | A+c | **B.** | A+C+B |
|  **C.** |  | **D.** | None |
| 13. If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output? |
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| **A.** | 1 | **B.** | 2 |
| **C.** | 7 | **D.** | 8 |

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| 14. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH, the gate is a(n): |
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| **A.** | AND | **B.** | NAND |
| **C.** | NOR | **D.** | OR |

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15. Which is correct grouping



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| **A.** | A | **B.** | B |
| **C.** | C | **D.** | D |

16. What logic function corresponds to the following circuit?



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| **A.** | *L =*(S1 OR S2) AND (S3 OR S4). | **B.** | *L =*S1 AND (S2 OR S3) AND S4 |
| **C.** | *L =*S1 OR (S2 AND S3) OR S4 | **D.** | *L =*(S1 OR S2) AND (S3 OR S4). |

17 number of switching functions of 3 variables is

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| **A.** | 8 | **B.** | 64 |
| **C.** | 128 | **D.** | 256 |

18. The Boolean expression can be minimized as



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| **A.** |  | **B.** |  |
| **C.** |  | **D.** |  |

19 the Boolean function AB+CD is to be realized using two input NAND gates. The minimum number of gates required is

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| --- | --- | --- | --- |
| **A.** | 2 | **B.** | 3 |
| **C.** | 4 | **D.** | 5 |

2o The logic expression is equal to

|  |  |  |  |
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| **A.** | A+B | **B.** | A+NOT B |
| **C.** | A-B | **D.** | NOT A + B |